Research on the Key Technology of Circuit Design of CMOS Pixel Sensors for High-speed Imaging

Yilin Zhang *

Institute of Frontier and Interdisciplinary Science, Shandong University, Qingdao China, China

* Corresponding Author Email: yilinzhang@mail.sdu.edu.cn

Abstract. In this paper, the CMOS pixel sensor for high-speed imaging is taken as the research object, and the key technologies and future development paths are discussed. In this study, we first analyze the requirements of high-speed imaging circuit design and the circuit architecture classification of high-speed CMOS pixel sensors, and focus on the design of high-speed readout circuits, including column-level parallel ADC architecture, pixel-level digitization circuits, and mixed-signal processing techniques. This paper mainly introduces noise suppression and high dynamic range circuits, including related double sampling (CDS) circuit optimization, noise suppression of global shutter, and dynamic range extension circuits, focusing on low power consumption and reliability design, involving near-threshold voltage circuit design and dynamic power consumption management. Finally, this study discusses the necessity of process-circuit-algorithm co-optimization, emphasizes the synergistic relationship between process and circuit, and proposes a future technology roadmap to achieve key breakthroughs in circuit design, which will provide important reference and guidance for the development of high-speed imaging.

Keywords: High-speed imaging, CMOS pixel sensor, Circuit design, Key technology.

1. Introduction

High-speed imaging technology plays a vital role in modern technology, and CMOS pixel sensors are widely used in various high-speed imaging systems due to their high integration, low cost, and easy manufacturing. However, with the increasing imaging speed and resolution, CMOS pixel sensors face a series of technical challenges [1-4]. First of all, noise suppression is one of the key technologies to improve image quality. In the process of high-speed imaging, electronic noise and thermal noise become the main factors affecting the image quality. Therefore, how to effectively suppress these noises and maintain the stability and accuracy of the signal is an important direction of current research. Second, high-speed imaging often requires a wide range of lighting conditions, which requires a wider dynamic range of CMOS pixel sensors. At present, the dynamic range can be effectively improved by improving the relevant dual sampling (CDS) circuit and adopting the global shutter technology, but there are still some limitations. In addition, low-power design is especially important for portable and embedded high-speed imaging devices. With the development of mobile devices and the Internet of Things, higher requirements are placed on the power consumption of CMOS pixel sensors. How to reduce power consumption while ensuring performance is a difficult point in current research [5], and with the increase in imaging speed, higher requirements are put forward for the circuit design of CMOS pixel sensors. This research focuses on the design of high-speed CMOS pixel sensor circuits, aiming to solve key challenges in high-speed imaging, including noise suppression, dynamic range extension, low-power design, and reliability optimization, and promote technological breakthroughs through process-circuit-algorithm collaborative optimization.

2. High-Speed Readout Circuit Design

2.1. Column-level Parallel ADC Architecture

The Analog-to-Digital Converter (ADC) architecture is a readout circuit design commonly used in high-speed CMOS pixel sensors, and its main purpose is to improve the speed and accuracy of data acquisition. In a column-level parallel ADC architecture, the analog signal of each pixel is first

converted to a digital signal, a process typically done by one or more analog-to-digital converters (ADCs). Since the data for each pixel needs to be converted independently, this architecture is particularly suitable for high-resolution imaging applications such as high-speed photography, video surveillance, etc. At the heart of the column-level parallel ADC architecture is how to efficiently process data from multiple pixels in parallel. To achieve this, a pipeline structure is often employed, where each stage is responsible for processing a portion of the data.

In practice, the performance of a column-level parallel ADC is affected by several factors, including sampling frequency, number of quantization bits, noise level, and power consumption.

Each stage in the column-level parallel ADC architecture is designed to ensure that data can be quickly and accurately converted to a digital format. In addition, to further improve the overall performance of the system, more advanced algorithms and techniques such as adaptive filtering, error compensation, etc., can also be considered to reduce the impact of noise and improve the dynamic range. Future research will further explore how this architecture can be optimized to meet more demanding application scenarios.

2.2. Pixel Level Digital Circuit

Pixel-level digitization circuits convert analog signals into digital signals for subsequent processing and analysis. This process involves a number of key technologies, including analog-to-digital converters (ADCs), sample-and-hold circuitry, and digital signal processors.

When designing pixel-level digitization circuits, the primary consideration is how to effectively improve the conversion speed and accuracy. This is typically achieved by optimizing the ADC architecture. For example, the use of high-bandwidth sample-and-hold circuitry can reduce signal loss during conversion, thereby improving the overall conversion efficiency. In addition, the use of multi-stage amplification and filtering technology can also effectively improve the quality of the signal, ensuring that the digitized data has high accuracy and reliability.

In practice, the design of pixel-level digitization circuits also needs to take into account power consumption and area limitations. As a result, researchers are constantly exploring new circuit topologies and materials to achieve the best balance between performance and power consumption. For example, the use of low-power logic gates and efficient power management strategies can significantly reduce the power consumption of the entire pixel sensor without sacrificing performance [6].

2.3. Mixed Signal Processing Technology

Mixed-signal processing technology combines the advantages of analog and digital circuits to achieve efficient processing of image data by precisely controlling the signal conversion process.

A typical example of mixed-signal processing is an analog-to-digital converter (ADC). The role of the ADC is to convert the analog signal into a digital signal for subsequent digital processing. In order to further improve the processing efficiency, the mixed-signal processing technology also adopts a variety of optimization strategies. For example, low-noise amplifiers (LNAs) are used to reduce the effects of front-end noise, multi-stage amplification is used to increase the dynamic range of the signal, and clock gating techniques are used to reduce unnecessary power consumption.

In addition, mixed-signal processing techniques include noise suppression and dynamic range extension. In terms of noise suppression, by introducing noise shaping technology, it is possible to effectively transfer noise energy from the useful signal frequency band to higher frequencies, thereby reducing the impact on the desired signal. Expansion of the dynamic range is achieved by increasing the linearity and dynamic range of the signal, which usually involves a nonlinear transformation of the signal.

Mixed-signal processing technology enables efficient and accurate processing of image data in high-speed CMOS pixel sensors by integrating the advantages of analog and digital processing.

3. Noise Suppression and High Dynamic Range Circuit

3.1. Correlated Double Sampling (CDS) Circuit Optimization

At the heart of the Correlation Double Sampling (CDS) circuit is the use of two samples to reduce the effect of noise during the readout process. In CMOS pixel sensors, the optimization of CDS circuitry is of great significance to improve image quality and extend dynamic range.

The basic principle of the CDS circuit is to sample the signal through two successive time windows, the first-time window is used to obtain the original signal and the second time window is used to obtain the reference signal of the background light. After the two signals are operated differently, the influence of background light can be effectively eliminated, so as to improve the signal-to-noise ratio of the signal. In order to further optimize the CDS circuit, the researchers proposed a series of improvement measures. For example, by adjusting the width and spacing of the sampling window, the signal characteristics under different lighting conditions can be better matched, resulting in better noise suppression. In addition, the use of more advanced analog front-end designs, such as the use of high-precision amplifiers and low-noise switches, can also significantly improve the overall performance of the CDS circuit.

In practical applications, the optimization of CDS circuits should not only consider the improvement at the hardware level, but also combine with the optimization at the algorithm level, such as adopting more efficient differential operation algorithms, so as to further improve the overall performance of the system. In addition, with the advancement of process technology, how to reduce power consumption while maintaining high performance is also an important direction of CDS circuit optimization.

3.2. Global Shutter Noise Suppression

Unlike traditional shutters, the global shutter exposes the entire image at the same time, avoiding motion blur and image distortion. However, the design of the global shutter faces the challenge of noise suppression, which directly affects the quality and clarity of the image.

In global shutter design, noise suppression is primarily concerned with electronic noise and thermal noise. Electronic noise typically originates from the sensor itself as well as the readout circuitry, while thermal noise is caused by temperature changes in the pixel element. In order to effectively suppress these noises, a variety of methods can be taken.

Electronic noise can be reduced by improving the structural design of the pixels, such as increasing the capacitance value or using more efficient photoelectric conversion materials. In addition, the use of low-noise transistors and resistors can also reduce noise levels. Thermal noise can be significantly reduced by controlling the temperature of the pixel elements through an effective heat dissipation system. This includes the use of efficient heat sinks, fans, or other cooling technologies. By introducing a noise filter into the readout circuit, the noise component can be effectively removed from the signal. This can be achieved through digital signal processing (DSP), which uses algorithms to analyze and filter the signal. By capturing multiple frames of images and calculating the average value, the effect of random noise can be effectively reduced. This method is particularly useful for scenes with a large dynamic range.

3.3. Dynamic Range Extension Circuit

The dynamic range extension circuit has a direct impact on the image quality. In high dynamic range (HDR) environments, the brightness of objects varies greatly, from the brightest to the darkest parts by orders of magnitude. In order to accurately capture details in this range, dynamic range extension circuitry needs to be able to efficiently handle a wide range of signals, from low to high light.

When designing dynamic range extension circuits, linear and logarithmic expansion are commonly used. Linear scaling is achieved with a simple amplifier whose gain can be adjusted for scenes where brightness does not change much. Logarithmic expansion, on the other hand, simulates the way the

human eye perceives light, and is more suitable for processing images with a large dynamic range. In practical applications, the circuit needs to automatically adjust its working state according to the specific input signal to ensure that the output image is neither overexposed nor underexposed, and maintains the best visual effect.

In addition, the design of dynamic range extension circuits involves several technical challenges, such as how to precisely control the degree of expansion, how to avoid nonlinear distortion, and how to ensure the stability and reliability of the circuit. Future research will pay more attention to the deep integration of circuits and algorithms to achieve higher performance and wider applications.

4. Low Power Consumption and Reliability Design

4.1. Near Threshold Voltage Circuit Design

With the continuous reduction of process nodes, the traditional threshold voltage operation mode cannot meet the needs of low power consumption and high performance. Near-threshold voltage operation can significantly reduce power consumption while maintaining transistor performance.

In high-speed imaging applications, CMOS pixel sensors need to reduce power consumption as much as possible while ensuring image quality. The core of the near-threshold voltage circuit design is how to reduce power consumption by optimizing the operating point of the transistor without affecting the image quality. Specifically, by adjusting the operating voltage of the transistor, lower power consumption can be achieved without sacrificing signal conversion efficiency.

When designing near-threshold voltage circuits, it is necessary to consider the selection of appropriate transistor types and configurations to adapt to different operating conditions and performance requirements. For example, with NMOS or PMOS transistors, the most appropriate configuration is selected according to the specific application scenario.

The power supply voltage needs to be set properly so that it can meet the performance requirements of the circuit and minimize power consumption. This usually involves dynamically adjusting the supply voltage to suit different operating states. In addition to hardware design, the optimization of signal processing algorithms is also an important means to reduce power consumption. The optimization algorithm can reduce unnecessary calculations and data transmission while ensuring the image quality.

4.2. Dynamic Power Management

In high-speed imaging applications, the power consumption of sensors is particularly prominent due to the increased demand for image processing. The core of dynamic power management is to adjust the power consumption of the circuit according to the actual operating state. For example, during image acquisition, when the sensor is static or inactive, it is possible to reduce the operating frequency of some circuits or turn off unnecessary function modules, thereby reducing power consumption. When high frame rates or high-resolution imaging are required, power consumption is increased accordingly to meet higher data processing requirements.

In order to control the power consumption more precisely, the working speed and power consumption of the circuit can be controlled by adjusting the supply voltage. Lower voltages can reduce power consumption, but at the same time affect the speed and stability of the circuit. In addition, the power consumption can be controlled by changing the operating frequency of the circuit. In cases where high-speed processing is not required, reducing the operating frequency can effectively reduce power consumption.

The implementation of dynamic power management relies on sophisticated control algorithms and efficient hardware support. In practice, dynamic power management needs to consider not only the balance between power and performance, but also cost and complexity. Therefore, designers need to simplify circuit design as much as possible and reduce unnecessary complexity to reduce manufacturing costs and power consumption without sacrificing performance. Future research will

focus more on how to further reduce power consumption while maintaining high performance to meet the growing demand for high-speed imaging.

5. Process-circuit-algorithm Collaborative Optimization

In the design process of high-speed imaging CMOS pixel sensors, the collaborative optimization between circuits, processes, and algorithms is the key to achieving high performance, low power consumption, and reliability. With the rapid development of imaging technology, the demand for CMOS pixel sensors is becoming more and more diverse, especially in the field of high-speed imaging. This has led to the pursuit of performance indicators such as high frame rate, large dynamic range, and low noise, which has put forward higher requirements for circuit design, process development, and algorithm implementation [7].

In the design of high-speed imaging CMOS pixel sensors, the co-optimization of process and circuit is the key to achieving high performance and low power consumption. This process involves every step from sensor design to the manufacturing process, and it is necessary to ensure that the circuit design can take full advantage of the advantages of the chosen process while overcoming its inherent limitations [8].

The co-optimization of process and circuit should select the most suitable semiconductor manufacturing process according to the needs of the target application. For example, for high-speed imaging applications, it may be necessary to select processes with high-mobility materials or special transistor structures to increase signal transmission speed and reduce noise.

For the circuit design, the circuit design should be based on the selected process characteristics. This includes, but is not limited to, the design of key circuit modules such as amplifiers, comparators, ADCs, and the interface design between these modules. By adjusting circuit parameters, such as gain, bandwidth, power consumption, etc., the circuit performance is optimized to meet the requirements of high-speed imaging. In terms of system integration, it is necessary to integrate the designed circuit modules into a complete system, considering the impact of layout, wiring, and other factors on the overall performance [9].

6. Future Technological Developments

In the field of high-speed imaging CMOS pixel sensors, the future technology roadmap will focus on improving the overall performance of the sensor, reducing power consumption, and enhancing reliability. With the advancement of technology, further optimization of high-speed readout circuits will become a key research direction, and the speed and accuracy of the serial-level parallel ADC architecture will be improved by adopting more advanced manufacturing processes and materials to meet the needs of higher frame rates and more complex image processing. At the same time, the innovative design of noise suppression and high dynamic range circuits will also be emphasized, and new noise suppression technologies and high dynamic range (HDR) circuits will be developed to reduce noise interference in the signal processing process and expand the dynamic range to achieve wider brightness and contrast performance. In addition, continuous improvement in low power consumption and reliability is another focus for future development, by exploring near-threshold voltage circuit designs and dynamic power management strategies to achieve lower power consumption and higher reliability in mobile and portable devices. Finally, the collaborative optimization of the process-circuit algorithm will be further strengthened, and the overall improvement of system performance will be achieved by integrating the advantages of process and circuit design, combined with the optimization of algorithms.

7. Conclusion

In the field of CMOS pixel sensors for high-speed imaging, achieving key breakthroughs in circuit design is an important driving force for the entire industry to move forward. Today, the main

challenges in circuit design include high bandwidth, low noise, high-speed conversion, and power consumption control. Through in-depth research and circuit architecture innovation, reducing noise interference, technological innovation to improve reliability and stability, exploring the deep integration of circuit design and image processing algorithms, and improving the overall system performance through algorithm-driven circuit design optimization looking forward to the future, with the continuous progress of new materials and production processes, the circuit design of CMOS pixel sensors will continue to develop towards higher performance, lower power consumption and greater flexibility. These breakthroughs will provide more options and greater application prospects for high-speed imaging, thereby promoting the wide application of related technologies.

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