

Development of Sobel Algorithm on FPGA

Ruifeng Hu

Department of Intelligent Medical Engineering, Shenzhen Technology University, Shenzhen, China
mail.stumail.sztu.edu.cn

Abstract. This paper introduces the implementation history of the Sobel algorithm on FPGA. Image edge detection is a basic technique in image processing and has extensive applications in various fields such as industry, medicine, aerospace, and the military. The speed of image processing has always been a challenging problem. The Sobel algorithm combines edge detection and smoothing operators, endowing it with good detection capabilities in many environments. Its capabilities are highly suitable for use in image detection. The Sobel algorithm is based on the spatial gradient of an image. By performing convolution operations on each pixel point, it calculates the gradient magnitude and direction of that point, thereby detecting the edge information in the image. As early as 2010, Zhang Lei and others developed specific algorithm principles and FPGA design architectures to achieve image edge detection. By 2016, Du Zhengcong and Ning Longfei introduced the idea of hardware acceleration and adopted the RAM + FPGA hardware structure to improve the processing speed. They also carried out modular design and modelling with the climbing method. The text also elaborates on the technological development process of the Sobel algorithm on FPGA and so on.

Keywords: Sobel Algorithm, Edge detection, FPGA.

1. Introduction

With the development of science and technology, the requirements for speed and real-time performance in image processing are increasing. Before that, there was Robert's operator, Prewitt's operator, Laplacian operator and so on. However, the Sobel operator stands out due to its advantages in aspects such as anti-noise performance and computational complexity. The Sobel algorithm is simple in calculation. By convolving the image in the horizontal and vertical directions, it can operate efficiently in real-time image processing to meet the current requirements. It has a relatively strong anti-noise ability. By performing weighted summation on the pixel neighbourhood, it can smooth out the noise and reduce its impact on edge detection. Because it mainly involves addition and multiplication operations, it is easy to implement on hardware and is widely used on hardware platforms such as FPGA [1]. In 2010, Zhang Lei and others achieved image edge detection with specific algorithm principles and FPGA design architectures, demonstrating that the Sobel algorithm in FPGA processes images faster than high-level programming languages such as C or C++ on software platforms. In the same year, Wenshuo Gao and others developed a method combining the Sobel edge detection operator and soft-threshold wavelet denoising to perform edge detection on images containing Gaussian white noise [2]. In 2016, Du Zhengcong and Ning Longfei put forward the idea of a hardware accelerator, and by controlling its operation, significantly improved the speed of real-time data processing [3]. In 2022, Li Fang and others, aiming at the problem of slow real-time processing speed in MATLAB, proposed the idea of hardware parallel computing. The results showed that the effect of implementing the edge detection algorithm with FPGA hardware was more favourable.

Through in-depth research on the mathematical model of the Sobel algorithm and the theoretical basis of image processing, the traditional Sobel operator algorithm was analysed and optimized. Improvements were made to aspects such as the gradient calculation method and filtering templates of the algorithm to enhance its accuracy and efficiency in edge detection. Meanwhile, in combination with relevant theoretical knowledge in the field of digital image processing, the algorithm was refined and enhanced at the theoretical level.

This paper verifies the highly efficient and comprehensive performance of implementing the Sobel operator with the idea of hardware acceleration on the FPGA platform, hoping to provide a reliable theoretical reference for subsequent research on image processing algorithms based on FPGA.

2. Principle of the Sobel Algorithm

2.1. The principle of the original Sobel algorithm

Sobel operator It is mainly used for edge detection. Technically, it is a discrete difference operator used to calculate the approximate value of the grey level of the image brightness function. Using this operator at any point in the image will generate the corresponding grey vector or its normal vector. The Sobel convolution factor is shown in Fig 1.

-1_{x1}	0_{x2}	$+1_{x3}$	$+1_{y1}$	$+2_{y2}$	$+1_{y3}$	P_1	P_2	P_3
-2_{x4}	0_{x5}	0_{x6}	0_{y4}	0_{y5}	0_{y6}	P_4	P_5	P_6
-1_{x7}	0_{x8}	-1_{x9}	-1_{y7}	-2_{y8}	-1_{y9}	P_7	P_8	P_9

Figure 1. The Sobel convolution factor

This operator contains two sets of 3x3 matrices, horizontal and vertical [4]. By performing a two-dimensional convolution of them with the image, the approximate values of the horizontal and vertical luminance differences can be obtained respectively. If A represents the original image, and G_x and G_y represent the grey values of the images after horizontal and vertical edge detection respectively, the formulas are as follows:

$$G_x = \begin{bmatrix} -1 & 0 & +1 \\ -2 & 0 & +2 \\ -1 & 0 & +1 \end{bmatrix} * A \text{ and } G_y = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix} * A \quad (1)$$

The horizontal and vertical grey values of each pixel in the image are combined through the following formula to calculate the magnitude of the grey value at that point [5].

$$G = \sqrt{G_x^2 + G_y^2} \quad (2)$$

Usually, to improve efficiency, an approximate value without taking the square root is used. However, this will lead to a loss of precision. When there is no other choice, it can be done as follows:

$$|G| = |G_x| + |G_y| \quad (3)$$

If the gradient G is greater than a certain threshold, then the point (x, y) is considered an edge point. Then the gradient direction can be calculated using the following formula (of course, if only edge detection is required, the direction does not need to be calculated).

$$\theta = \arctan\left(\frac{G_y}{G_x}\right) \quad (4)$$

2.2. Improved Sobel Algorithm

The original Sobel algorithm is simple and easy to implement, but because the algorithm only detects the horizontal and vertical layers, the edge detection may be misjudged in complex images. In "An Improved Sobel Edge Algorithm and FPGA Implementation", the method of increasing the layer detection direction is used to solve the problem of edge misjudgement in complex images [6]. The improvement idea is to increase the two directions of 45° and 135°, that is, to compare with all the pixels around the selected pixel. The results show that the improved Sobel algorithm is more in line with the requirements of modern high-definition complex image detection.

3. Introduction to FPGA

FPGA (Field Programmable Gate Array) is a programmable semiconductor device, which contains many programmable logic units (CLB), which can be used to implement complex digital circuit design [7]. FPGA has the following characteristics:

Strong parallel processing capability: multiple logic units can work simultaneously, making it suitable for high-performance computing.

Flexibility: It can be programmed in a hardware description language (HDL) to achieve different functions.

Good real-time performance: Low latency, suitable for real-time applications.

Rich resources: including DSP blocks, block RAM, high-speed IO interfaces, etc.

The internal structure of an FPGA typically includes:

Programmable logic unit (CLB): used to implement basic logic operations and storage functions.

Embedded memory (Block RAM): used to store data and intermediate results.

Digital signal processing unit (DSP): used to realize complex operations such as multiplier and accumulator.

Input-output unit (IO): used for data exchange with external devices.

Clock Management Unit (CMT): Used for the distribution and management of clock signals.

4. Application of Sobel on FPGA

4.1. Introduction to Edge Detection Algorithm

In computer vision and image processing, edge detection concerns the localization of significant variations of the grey-level image and the identification of the physical phenomena that originated them [8]. The so-called edge refers to the collection of pixels around which the grey release changes sharply, and it is the most basic feature of the image. The edge exists between the target, background and area, so it is the most important basis for image segmentation. Since the edge is a sign of position and is not sensitive to changes in the grey release, therefore, the edge is also an important feature of image matching [9]. Edge detection and region division are two different methods of image segmentation, and they have complementary characteristics. In edge detection, it is to extract the features of discontinuous parts of the image and determine the area according to the closed edge. In region division, the image is divided into areas with the same characteristics, and the boundary between the areas is the edge. Since the edge detection method does not need to divide the image pixel by pixel, it is more suitable for the segmentation of large images. The edge can be roughly divided into two types, one is a step-like edge, where the grey release value of the pixels on both sides of the edge is different; the other is a roof-like edge, where the edge is at the turning point where the grey release value changes from small to large too small. The main tool for edge detection is the edge detection template. There are many edge detection, typical edge detection technologies such as Sobel operator, Privette operator, and Roberts cross edge detection.

4.2. The initial application of the Sobel algorithm on FPGA

In the paper "Digital Image Edge Detection and FPGA Implementation Based on Sobel Operator" by Zhang Lei et al. in 2010, the Sobel edge detection operator combines edge detection and smoothing operators to make it have good detection ability in noisy environments. Choosing different smoothing methods will have different image-sharpening results. In this paper, the first-order partial derivative is expressed by the first-order difference approximation, and the edge detection is realized by layer calculation of the image. Image edge enhancement is usually high-pass filtering, and image sharpening enhances the high-frequency part of the image spectrum, which is equivalent to subtracting its low-frequency component from the original image. In this implementation, the FPGA design architecture is for the input of 8 8-bit pixel values to be compared by layer through 8-byte bus and 8-bit starting value [10]. According to the value provided by the 8-bit input of the threshold, the

output of this scheme is the edge detection pixel value in the form of 8-bit zeros or 8-bit 255-pixel values. The modules that make up this architecture are the decrypt or module, the final addition and division module and the comparison module. The simulation results show that the chip can run at 134MHz, and satisfactory edge detection results are obtained within 7.8ms through the experiment of 1024 * 1024-pixel size images. The FPGA uses XilinxSpartan3 XC3S50-5PQ208, and its chip utilization is only 26% of the total resources. The Spartan-3 FPGA offers the ideal combination of performance and flexibility to meet the requirements of standard and high-resolution image processing, video analysis, multi-channel video coding, and more, for faster and more efficient video transmission.

4.3. Application of Improved Sobel on FPGA

In 2024, Wang Zishuo et al. published "Improved Edge Algorithm and Its FPGA Implementation" [11]. In this paper, given the lack of adaptability and poor real-time performance of the traditional edge detection algorithm implemented on FPGA, combined with the characteristics of high-speed parallel processing of FPGA data, an improved edge detection algorithm is proposed. The algorithm in the experiment firstly applies bilateral filtering to the Canny edge detection algorithm to reduce noise while preserving the image edge layer information; secondly, the improved Sobel operator is used to calculate the amplitude of the layer in four directions to improve the positioning accuracy of the image edge. In this experiment, the experimenter changed the original 2×2 operator to the 3×3 Sobel operator and added the amplitude calculation of 45° and 135° directions. This also improves the performance. The double threshold segmentation of the Canny algorithm is used to further process the weak edge pixels between the high and low thresholds of the image layer, connecting the strong edge and the weak edge adjacent to it. In this experiment, an industrial camera with the main control chip of Artix-7 series FPGA is used as the hardware platform to implement the adaptive Canny edge detection algorithm, and the performance of the algorithm in hardware processing is tested. The Sobel algorithm and the Canny algorithm are used in this experiment, and the PSNR value of the experimental algorithm is improved by 41.7%. Compared with the previous 3×3 and 5×5 Gaussian filters, the PSNR value of the algorithm is improved by 109% respectively, showing a significant improvement effect. Even if more and more different algorithms appear in the future, the Sobel algorithm is highly likely to work simultaneously to achieve higher data processing efficiency.

5. Conclusion

The implementation of the Sobel algorithm on FPGA also faces problems, such as limited hardware resources: the logic resources inside the FPGA are limited. When the Sobel algorithm is implemented on FPGA, many multipliers and adders are required to complete the convolution operation. At the same time, to store image data and intermediate results, it also needs to occupy a certain storage unit. When processing high-resolution images, it is easy to run out of resources, which will affect the processing speed. The contradiction between processing speed and resource consumption: To improve the processing speed of the Sobel algorithm on FPGA, it may be necessary to adopt a parallel computing structure to increase the number of processing units. However, this will lead to a significant increase in the usage of hardware resources and also bring higher power consumption. However, if too much emphasis is placed on resource conservation, the use of fewer processing units and lower clock frequencies will result in processing speeds that cannot meet real-time requirements.

The implementation of the Sobel algorithm on FPGA has experienced many years of development and achieved remarkable results. The application of the Sobel operator on FPGA continues to expand and deepen.

In the early days, such as the research of Zhang Lei and others in 2010, FPGA has been used for digital image edge detection. Through the principle of the Sobel algorithm and FPGA design architecture, image edge detection has been realized, and ideal results have been achieved.

In 2016, Du Zhengcong and Ning Longfei's research introduced the idea of hardware accelerators. The processing speed of the algorithm was greatly improved through pipeline design and ping-pong operation.

In conclusion, the implementation of Sobel operators on FPGAs has achieved fruitful results and made important contributions to the development of the field of digital image processing. The implementation of Sobel algorithms on FPGAs can not only make full use of its parallel processing capabilities to achieve real-time image processing but also optimize resource utilization and power consumption under the premise of ensuring processing speed and accuracy through reasonable system architecture design and optimization. In the future, with the continuous development of FPGA technology, the performance and flexibility of image processing can be further improved to meet more complex and diverse application requirements.

This report details the development process of the Sobel algorithm implemented on FPGA. Hope this report can provide a valuable reference for those engaged in related research and development.

References

- [1] ZHANG Lei, YANG Wei-ming, ZONG Ai-hua, LI Zi-yi; the Edge Detection of Digital Image and its realization by FPGA technique based on Sobel operator.
- [2] Wenshuo Gao; Xiaoguang Zhang; Lei Yang; Huizhong Liu. An improved Sobel edge detection. 2010 3rd International Conference on Computer Science and Information Technology, 09-11 July 2010.
- [3] Du Zhengcong, Ning Longfei. Image edge detection based on Sobel algorithm in FPGA implementation [J]. Application of Electronic Technique, 2016, 42 (10): 89-91, 95.
- [4] Lili Han, Yimin Tian and Qian hui Qi, Research on edge detection algorithm based on improved sobel operator, 2019 International Conference on Computer Science Communication and Network Security, MATEC Web Conf. Volume 309, 2020.
- [5] O. R. Vincent, O. Folorunso; A Descriptive Algorithm for Sobel Image Edge Detection; Proceedings of Informing Science & IT Education Conference (InSITE) 2009.
- [6] Kun Zhanga, Yuming Zhangb, Pu Wangc, Ye Tiand, Jun Yang. An Improved Sobel Edge Algorithm and FPGA Implementation. Procedia Computer Science 131, 2018, 243–248.
- [7] N. Nausheen, A. Seal, P. Khanna, S. Halder, “A FPGA based implementation of Sobel edge detection,” Science Direct, Microprocessors and Microsystems, 56, 2018, pp. 84-91.
- [8] Ziou et al. Edge detection techniques - an overview Int. J. Pattern Recognit. Image Anal. (1998)
- [9] I. Yasri, N. H. Hamid, and V. V. Yap, “Performance analysis of FPGA based Sobel edge detection operator,” 2008 International Conference on Electronic Design, Dec. 2008, doi: 10.1109/ICED.2008.4786751.
- [10] Z. Xiangxi, Z. Yonghui, Z. Shuaiyan, Z. Jian, “FPGA implementation of edge detection for Sobel operator in eight directions”, In Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems, Chengdu. 2018, pp. 520-523.
- [11] Wang Zishuo, SHAN Yanhu, CHU Chengqun, CHENG Hongtao, GAO Xin, ZHAO Xinglong; Improved edge detection algorithm and its FPGA implementation 10. 14016/j. cnki. jgzz. 2024. 03. 074.